REMARKS

Applicants have reviewed the comments and rejections set forth by the Examiner in the Office Action dated July 10, 2005 and respectfully respond with the amendments above and the arguments set forth below. Applicants respectfully thank the Examiner for acknowledging Applicants' election of Claims 1-12. Claims 1-6 and 10 are pending in the above captioned matter. Claims 7-9 and 11-12 are cancelled herein. (Claims 13-21 have been previously cancelled.) No new matter is added herein. Applicants respectfully request reconsideration in view of the above amendments and the following arguments.

CLAIM REJECTIONS

35 USC §112

Claim 2 is rejected under 35 USC 112 (¶2), for insufficient antecedent basis for the term "said active component." As amended herein, Claim 2 reads as shown below, with underlining added for emphasis.

> 2. The semiconductor structure as recited in Claim 1 wherein said active device comprises a transistor.

As amended herein, Claim 2 recites --said active device,-- which has antecedent basis in Claim 1. Applicants respectfully assert that, as amended herein, Claim 2 is allowable under 35 USC 112.

35 USC §102

Claims 1-2 and 7-9 are rejected under 35 USC 102(b) over World Intellectual Property Organization (WIPO) Patent Cooperation Treaty (PCT) application publication no. WO 00/35013 by Kloen, et al. (hereinafter Kloen). Applicants have reviewed the reference cited and respectfully assert it does not

teach or suggest the embodiments of the present invention as recited in Claims 1-2 and 7-9 for the following rationale.

Claims 7-9 are cancelled herein. Thus, Applicants respectfully assert that their rejection under 35 USC 102(b) is moot. With respect to Claims 1-2, Applicants respectfully assert the argument set forth below.

As Applicants understand the reference, Kloen teaches an integrated circuit (IC) device wherein bond pads are disposed substantially over an active circuit. The teaching of Kloen thus differs from the embodiments of the present invention recited in Claims 1-2.

As amended herein, Claim 1 reads as shown below, with underlining added for emphasis.

> 1. A semiconductor structure comprising:
> a pad area wherein said pad area comprises:
> a substrate;
> a first layer of metal disposed above said substrate wherein said active device is disposed below said first layer of metal;
> a second layer of metal disposed above said first layer of metal;
> a layer of dielectric disposed between said first metal layer and said second metal layer;
> a via disposed within said dielectric layer wherein said via electrically couples said first and said second metal layer; and
> one or more subsequent layers of metal between said first and said second metal layers, wherein said <u>via comprises one or more of a plurality of vias and wherein one or more of said vias electrically couples one or more of said subsequent layers with one or more of each other, said first and said second layers of metal</u>; and
> an active device of said semiconductor structure disposed below said pad area and within said substrate wherein <u>one or more of said vias electrically couples said active device with one or more of said metal layers</u>.

Independent Claim 10 is amended herein after a similar fashion. Claims 2 and 7-9

depend on independent Claim 1.

As amended herein, independent Claims 1 and 10 recite that a via disposed within a dielectric layer of the semiconductor structure electrically couples first and second metal layers, that one or more layers of metal are disposed between the first and second metal layers, that the via comprises one or more of a plurality of vias, that one or more of the vias electrically couples one or more of the subsequent layers with one or more of each other, the first and the second layers of metal, that an active device of the semiconductor structure, disposed below its pad area and within the substrate and that one or more of the vias electrically couples the active device with one or more of said metal layers. This is explained in the original specification , for instance from line 11 at page 5 through line 12 at page 7.

Disposing one or more metal layers between the first and second metal layers, interconnecting the active device, disposed in substrate directly beneath the pad area, with one or more of the first, second and interspersed metal layers with one or more of multiple vias, and interconnecting one or more of the first, second and interspersed metal layers with one or more of multiple vias, as recited in Claims 1 and 10 herein has the benefit of allowing great flexibility in design, layout, fabrication, and functionality. Disposing active devices directly beneath the pad area has the benefit of efficient use of available substrate. Both of these benefits provide advantages relating to efficiency, productive yield and economy.

Applicants find no teaching or suggestion in Kloen directed towards one or more layers of metal are disposed between the first and second metal layers, towards the via comprising one or more of a plurality of vias, towards one or more of the vias electrically coupling one or more of the subsequent layers with one or more

of each other, the first and the second layers of metal, towards an active device of the semiconductor structure, disposed below its pad area and within the substrate, which is coupled with one or more of the vias to with one or more of said metal layers, as recited in the claimed embodiments herein.

On the contrary, Kloen expressly teaches only two layers of metal between the pad area and the active device there under, as clearly described and shown with reference to Kloen's Figure 2. This teaches way from the claimed embodiments recited herein, which relate to one or more layers of metal are disposed between the first and second metal layers, towards the via comprising one or more of a plurality of vias, towards one or more of the vias electrically coupling one or more of the subsequent layers with one or more of each other, the first and the second layers of metal, towards an active device of the semiconductor structure, disposed below its pad area and within the substrate, which is coupled with one or more of the vias to with one or more of said metal layers.

Thus, Applicants respectfully assert that Kloen does not teach, suggest or anticipate the claimed embodiments recited herein, teaches away there from, and thus provides no motivation to produce these claimed embodiments. Therefore, Applicants respectfully assert that Claims 1-2 are allowable over the cited reference under 35 USC 102(b).

35 USC §103

Claims 3-6 and 10-12 are rejected under 35 USC 103(a) over Kloen. Applicants have reviewed the reference cited and respectfully assert that it does not teach or suggest the embodiments recited in Claims 3-6 and 10 for the following rationale.

Claims 11-12 are cancelled herein. Thus, Applicants respectfully assert that their rejection under 35 USC 103(a) is moot. With respect to Claims 3-6, Applicants respectfully assert the argument set forth below.

Applicants respectfully repeat and re-assert the argument set forth above in regard to the Kloen reference, as applied to Claim 1. Claims 3-6 depend upon independent Claim 1, which is amended herein after a similar fashion as is Claim 10.

As amended herein, independent Claims 1 and 10 recite that a via disposed within a dielectric layer of the semiconductor structure electrically couples first and second metal layers, that one or more layers of metal are disposed between the first and second metal layers, that the via comprises one or more of a plurality of vias, that one or more of the vias electrically couples one or more of the subsequent layers with one or more of each other, the first and the second layers of metal, that an active device of the semiconductor structure, disposed below its pad area and within the substrate and that one or more of the vias electrically couples the active device with one or more of said metal layers. This has benefits and advantages as explained above.

Applicants find no teaching or suggestion in Kloen directed towards one or more layers of metal are disposed between the first and second metal layers, towards the via comprising one or more of a plurality of vias, towards one or more of the vias electrically coupling one or more of the subsequent layers with one or more of each other, the first and the second layers of metal, towards an active device of the semiconductor structure, disposed below its pad area and within the substrate,

which is coupled with one or more of the vias to with one or more of said metal layers, as recited in the claimed embodiments herein.

On the contrary, Kloen expressly teaches only two layers of metal between the pad area and the active device there under, as clearly described and shown with reference to Kloen's Figure 2. This teaches way from the claimed embodiments recited herein, which relate to one or more layers of metal are disposed between the first and second metal layers, towards the via comprising one or more of a plurality of vias, towards one or more of the vias electrically coupling one or more of the subsequent layers with one or more of each other, the first and the second layers of metal, towards an active device of the semiconductor structure, disposed below its pad area and within the substrate, which is coupled with one or more of the vias to with one or more of said metal layers.

Thus, Applicants respectfully assert that Kloen does not teach, suggest or anticipate the claimed embodiments recited herein, teaches away there from, and thus provides no motivation to produce these claimed embodiments. Therefore, Applicants respectfully assert that Claims 3-6 and 10 are allowable over the cited reference under 35 USC 103(a).

CONCLUSION

By the rationale set forth above, Applicants respectfully assert that Claim 2 is allowable under 35 USC 112 (¶2). By the rationale set forth above, Applicants also respectfully assert that Claims 1-2 are allowable over the cited reference under 35 USC 102(b). Further, by the rationale set forth above, Applicants respectfully assert that Claims 3-6 and 10 are allowable over the cited reference under 35 USC 103(a).

Accordingly, Applicants respectfully request that the rejection of Claim 2 under 35 USC 112(¶2), of Claims 1-2 under 35 USC 102(b) and of Claims 3-6 and 10 under 35 USC 103(a) be withdrawn and that Claims 1-6 and 10 be allowed.

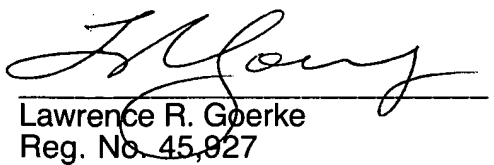
The Examiner is invited to contact Applicants' undersigned representative if the Examiner believes such action would expedite resolution of the present Application.

Please charge our deposit account No. 23-0085, for any unpaid fees.

Respectfully submitted,

WAGNER, MURABITO & HAO, LLP

Dated: Sept. 9, 2005



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